REMARKS

The claims remaining in the present application are Claims 1-20. The Examiner is thanked for performing a thorough search. None of the claims have been amended.

CLAIM OBJECTIONS

Claims 16 and 19

The Office Action asserted that lines 11 and 14 of Claim 16 and line 3 of Claim 19 should be changed from "updator" to "updater." Applicant respectfully traverses. The MPEP states that Applicants are their own lexicographers. Applicant has invented a noun form of the verb "to update." The use of "or" instead of "er" clearly indicates that this is a noun form. Applicant used "updator" consistently through the specification and the claims. The term "updator" is not inconsistent with the usual meaning of "to update." For at least these reasons, Applicant believes that this objection has been addressed.

35 U.S.C. §102

Claims 1 and 3-8

Claims 1 and 3-8 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,347,372 by Takashima et al. (referred to hereinafter as "Takashima"). Applicants respectfully submit that embodiments of the present invention are neither taught nor suggested by Takashima.

Claim 1 recites.

A method of providing updated processor polling information, comprising:

collecting processor polling information at boot time to be provided to an operating system, said processor polling information describing operating conditions of an integrated processing system;

notifying said operating system that a triggering event has occurred, wherein said triggering event potentially alters said operating conditions of said integrated processor system; and

providing updated processor polling information during runtime to said operating system, said updated processor polling information reflecting operating conditions of said integrated processor system after the occurrence of the triggering event.

Applicant respectfully submit that Takashima does not teach or suggest any of the limitations "collecting processor polling information at boot time to be <u>provided to an operating system</u>, said processor polling information describing operating conditions

Serial No. 10/737,111 Art Unit 2113 Examiner: Mehrmanesh, Elmira - 2 - 200313534-2 of an integrated processing system; <u>notifying said operating system</u> that a triggering event has occurred, wherein said triggering event potentially alters said operating conditions of said integrated processor system; and providing updated processor polling information <u>during runtime</u> to said operating system, said updated processor polling information reflecting operating conditions of said integrated processor system after the occurrence of the triggering event," (emphasis added) as recited by Claim 1

Referring to the last sentence of the abstract, Takashima teaches loading boot data into a boot processor via a shared bus. For example, the abstract states from line 6 to the last line of the abstract,

The processors constitute at least one boot processor to which the boot data is to be loaded. The boot control device includes a time slot division unit which produces time slots on the shared bus by multiplexing channels for the processors, and a time sharing control unit which determines a time slot for the boot processor among the time slots produced, and assigns the time slot to the boot processor. The time sharing control unit includes a processor interface part which notifies a time-slot location of the time slot determined, to the boot processor. A bus time-slot setting part notifies the time-slot location to the storage device, allowing reading of the boot data from the storage device and inserting of the boot data into the time slot at the time-slot location among the time slots on the shared bus, so that the boot data is loaded into the boot processor via the shared bus. (emphasis added)

The Office Action asserted that Takashima teaches "collecting processor polling information at boot time to be <u>provided to an operating system</u>, said processor polling information describing operating conditions of an integrated processing system," (emphasis added) at element 36 on FIG. 4. Referring to FIG. 4, element 36 is a polling control unit (POLC) which is a part of the boot control device 45. Col. 6 lines 34-39 clearly indicates that the boot control device 45 is a piece of hardware. There is nothing in Figure 4 or anywhere in Takashima that indicates that Takashima teaches "collecting processor polling information at boot time to be <u>provided to an operating system</u>." Therefore Takashima does not teach or suggest "collecting processor polling information at boot time to be <u>provided to an operating system</u>, said processor polling information describing operating conditions of an integrated processing system," (emphasis added) as recited by Claim 1.

The Office Action asserted that Takashima teaches "notifying said operating system that a triggering event has occurred, wherein said triggering event potentially

Serial No. 10/737,111 Examiner: Mehrmanesh, Elmira Art Unit 2113 200313534-2 alters said operating conditions of said integrated processor system," at Col. 8 lines 2-9. Col. 8 lines 2-9 state,

When an error occurs in one of the "N" processors of the processor block 31, the <u>CC 41</u> notifies the <u>TSC 33</u> that the TSC 33 should avoid the assignment of the time slot to the defective processor. The CC 41 causes the TSC 33 to notify <u>a host system</u>, which manages the processor of concern, that the channel for the processor of concern is defective, or that the channel for the processor of concern should be set in an OFF status. (emphasis added).

It is not clear to Applicant what in Col. 8 lines 2-9 the Office Action asserts teaches an "operating system." The CC 41 and the TSC 33 are a part of the boot control device 45 which as already established herein is a piece of hardware. Takashima does not clarify what his "host system" is. Referring to the abstract, Takashima teaches loading boot data into a boot processor via the shared bus. Therefore, Takashima's host system is clearly not the operating system. Further, Col. 9 lines 12-13 state, "Next, the TSC 33 notifies a boot start timing...," which occurs after the processing described Col. 8 lines 2-9. Col. 8 lines 2-9, which refers to notifying a "host system." Part of the boot process is to boot the operating system. Therefore, the operating system cannot be notified of anything until the boot process has completed. Since Col. 9 lines 12-13 indicate that the boot process has not completed yet, the "host system" cannot be an operating system or a part of an operating system because the boot process hasn't completed yet.

The Office Action asserts that Takashima teaches "providing updated processor polling information during runtime to said operating system, said updated processor polling information reflecting operating conditions of said integrated processor system after the occurrence of the triggering event," (emphasis added) at Col. 7 lines 43-47 and Col. 7 lines 26-42. Col. 7 lines 43-46 states, "The external port interface unit (EX/IF) 38 sends an external signal to the storage device 42 in order to update the information stored in the storage device 42" (emphasis added). Note that Col. 7 lines 43-46 say nothing about an operating system or during run time. Clearly the storage device 42 is not an operating system. Further Col. 7 lines 26-42 say nothing about an operating system or during run time, among other things. Col. 7 lines 26-42 refer to a POLC 36, a TSC 33 and a P/SD 35, which are all apart of the boot control device 45. As already established the boot control device 45 is hardware not an operating system.

Serial No. 10/737,111 Examiner: Mehrmanesh, Elmira Art Unit 2113 200313534-2

For the foregoing reasons, Claim 1 should be patentable. Claims 2-8 depend on Claim 1. These dependent claims include all of the limitations of their respective independent claims. Further, these dependent claims include additional limitations which further make them patentable. Therefore, these dependent claims should be patentable for at least the reasons that their respective independent claims should be patentable.

Claims 9-20

Claims 9-20 are rejected under 35 U.S.C. §102(e) as being anticipated b6y U.S. Patent No. 6,948,094 by Schultz et al. (referred to hereinafter as "Schultz"). Applicants respectfully submit that embodiments of the present invention are neither taught nor suggested by Schultz.

Claim 9 recites,

A computer program embodied on a computer readable medium for providing updated processors <u>polling</u> information, the computer program causing a computer to perform the steps of:

creating a processor <u>polling</u> information table, said processor <u>polling</u> information table being populated with boot time processor <u>polling</u> information, wherein said processor <u>polling</u> information describes operating conditions of an integrated processing system; and

updating said processor <u>polling</u> information table upon receipt of a notification that a triggering event has occurred, wherein said triggering event may potentially alter said operating conditions of said integrated processor system. (emphasis added).

Applicant respectfully submits that Schultz does not teach or suggest any of the limitations of Claim 9.

Schultz teaches a method of correcting a machine check error based on the interrupt model. For example, referring to Col. 3 lines 32-46, Schultz states,

...When the platform or processor hardware 101 generates a machine check 200, control is passed to a processor error handler 204 in the PAL 104. In turn, control is passed to the platform error handler 206 in the SAL 106. Control may in turn be passed to the OS machine check handler 206 in the SAL 106. Control may in turn be passed to the OS machine check handler 10 in the operating system software 110. If the error is corrected, control will be returned to the interrupted processor context. Otherwise, the system will be halted or rebooted.

The <u>machine check architecture error handling model</u> consists of different software components that work in close cooperation to handle different error conditions. <u>PAL, SAL, and the operating system have error handling components, which are tightly coupled</u> through a well defined interface.

Serial No. 10/737,111 Examiner: Mehrmanesh, Elmira Art Unit 2113 200313534-2

Machine checks are a type of interrupt. Col. 3 lines 32-46 clearly state that PAL, SAL and the operating system are tightly coupled through the use of an interrupt type model.

In contrast, Claim 9 recites "polling," which is fundamentally different from an interrupt. The instant application serial no. 10/737,111 explains this fundamental difference starting in the last paragraph on page 5 through the second paragraph on page 6. In referring to this portion of the instant application, Applicant is not attempting to read portions of the instant application into the claims. Claim 9 clearly recites "polling." Applicant is merely providing the Examiner with information so that the Examiner can understand the fundamental difference between polling, which Claim 9 recites, and interrupts, which Schultz teaches.

For the forgoing reasons, Claim 9 should be patentable. Claim 16 should be patentable for at least the reason that Claim 16 also recites "polling." Claims 10-15 depend on Claim 9. Claims 17-20 depend on Claim 16. These dependent claims include all of the limitations of their respective independent claims. Further, these dependent claims include additional limitations which further make them patentable. Therefore, these dependent claims should be patentable for at least the reasons that their respective independent claims should be patentable.

Serial No. 10/737,111 Art Unit 2113 Examiner: Mehrmanesh, Elmira - 6 - 200313534-2

CONCLUSION

In light of the above listed amendments and remarks, reconsideration of the rejected claims is requested. Based on the arguments and amendments presented above, it is respectfully submitted that Claims 1-20 overcome the rejections of record. For reasons discussed herein, Applicant respectfully requests that Claims 1-20 be considered be the Examiner. Therefore, allowance of Claims 1-20 is respectfully solicited.

Should the Examiner have a question regarding the instant amendment and response, the Applicant invites the Examiner to contact the Applicant's undersigned representative at the below listed telephone number.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Dated: 3/2/___, 2007

John P. Wagner Jr.

Registration No. 35,398

Address:

Westridge Business Park

123 Westridge Drive

Watsonville, California 95076 USA

Telephone:

(408) 938-9060 Voice (408) 234-3749 Direct/Cell (408) 763-2895 Facsimile

Serial No. 10/737,111

Examiner: Mehrmanesh, Elmira

Art Unit 2113 200313534-2